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14ELD24

Second Semester M.Tech. Degree Examination, June/July 2015
Real Time Operating Systems

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. What is response time of a real time service? Draw and explain the real time service timeline. **(08 Marks)**

b. Using service utility function differentiate between the following. Also give an example for each:
   i) Hard real-time service and isochronous service.
   ii) Soft real-time service and anytime service. **(08 Marks)**

c. List any four key features that an RTOS should have. **(04 Marks)**

2 a. What is thread safe reentrant function? Write a C program as s global function and make it thread safe. **(04 Marks)**

b. Check whether the following set of 3 periodic tasks are schedulable under RM on a uniprocessor using RM LUB test where service
   S_1 has $C_1 = 20$, $T_1 = 100$
   S_2 has $C_2 = 30$, $T_2 = 150$
   S_3 has $C_3 = 90$, $T_3 = 200$. **(06 Marks)**

c. Why RMLUB is sufficient test? Prove RM LUB mathematically. **(10 Marks)**

3 a. Write the relation for scheduling point test and completion test. In a set of three services test whether service S_3 is feasible using scheduling point test. Where
   S_1 has $C_1 = 10$, $T_1 = 40$
   S_2 has $C_2 = 15$, $T_2 = 60$
   S_3 has $C_3 = 20$, $T_3 = 120$
   Write all inequality expressions. **(10 Marks)**

b. Based on which parameter priorities are assigned to services in following scheduling policies:
   i) RM ii) DM iii) EDF iv) LLF. **(04 Marks)**

c. Compare overload condition in RM and EDF scheduling policies with schematic diagram. **(06 Marks)**

4 a. Write the overlapping conditions for CPU and I/O time relative to S_i and D_i. **(05 Marks)**

b. Draw four stage pipeline and list any two pipeline hazards. **(05 Marks)**

c. Determine WCET and ACET of a real time service in a system with following characteristics. Memory latency is 12 clock cycles, I/O latency 60 clock cycles, NOA is 0.6. It receives 10000 frames for processing where each frame has 2120 instructions. Expected path instruction count per frame is 1850. Expected cache miss is 38%. Cache penalty is 14 clock cycles. CPI effective for all cases is 2. Clock frequency of system is 100MHz. If the above system is Hard real-time system if the total interference to service 'i' is 100ms, and if deadline of service 'i' is 1.2 sec can the service meet its deadline? **(10 Marks)**

5 a. Draw the memory map of direct mapped cache fully associative cache and 2-way-associative cache. Write advantage and drawback of each of them. **(06 Marks)**

b. An ECC of memory interface is based upon hamming code. Encode the data "10111100". Detect and tabulate conditions for SBE, MBE and parity error. **(10 Marks)**

c. Determine availability and QoS of a RTS which has MTBF = 18 mins, MTTR = 4 mins service dropouts are 32 among 105 deliveries. **(04 Marks)**

6 a. Explain unbounded priority inversion with an example. Explain two techniques to overcome it with relevant sketch and example. **(08 Marks)**

b. Draw the scheduling diagrams for RM, EDF and LLF policies for the following set of services:
S_1 has $C_1 = 1$ $T_1 = 2$
S_2 has $C_2 = 1$ $T_2 = 4$
S_3 has $C_3 = 4$ $T_3 = 16$ **(08 Marks)**

c. Draw the schematic and explain the device driver firmware interface. **(04 Marks)**

7 a. Explain the message queue and heap-based message queue for inter task communication. **(06 Marks)**

b. Explain method to find path length, efficiency and calling frequency using C code to compute Fibonacci sequence. **(07 Marks)**

c. Explain 3 levels of single step debugging and 2 ways of breakpoint implementation. **(07 Marks)**

8 a. What is assertion in debugging RTS program? Give an example. **(04 Marks)**

b. Explain reliability and availability, their similarities and differences. **(08 Marks)**

c. Describe RTOS design issues in PIC controller. **(08 Marks)**

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